Ka-Band 2 Watt Power SSPA for LMDS Application

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ABSTRACT

A Ka-band high power, single power supply SSPA using mm wave power PHEMT process has been successfully developed for LMDS (Local Multi-point Distribution System) application. Operated under 5V single power supply, this four stage amplifier has 23dB of linear gain and typical 33 dBm (2W) of 1dB gain compression power for the entire 900 MHz bandwidth (27.5 ~ 28.4 GHz). This amplifier is designed to meet the demanding hub station linearity requirement of DAVIC specification for grade A QPSK modulation of data and video transmission. When operated at 30dBm (1W) power output with single channel band limited signal, the spectral re-growth is -35dBc, 3dB better than the -32dBc performance target. To our knowledge, the linearity performance presented is the best reported so far for this application.

INTRODUCTION

Recent emerging commercial wireless applications have significantly increased the need for high power amplifiers in the millimeter wave frequency range. Specifically the applications include high data rate point to point digital radios at 23, 26, & 38 GHz, point to multi-point LMDS at 28 GHz, and Ka band VSAT terminals at 30 GHz. Needs for higher spectral efficiency drives the use of higher levels of modulations like QPSK, 16 QAM, & 64 QAM which in turn necessitates high linearity amplifiers to be used at the output of the transmitters. Power level requirements, depending on the application, vary from 0.5W to greater than 2W. This paper describes a high linearity 2W amplifier designed specifically for the US LMDS hub transmitter application [Ref.1]. This amplifier uses a mm wave high performance power PHEMT device. The design approach and devices can be easily adopted for point-to-point as well as satellite power amplifier applications.

SEMICONDUCTOR PROCESS DESCRIPTION

Product development started with GaAs process improvement. The proprietary high performance power PHEMT process is an improved version of the process previously developed for mm wave satellite communication program [Ref.2]. Double doped AlGaAs/InGaAs epi material is grown using in-house MBE capability. Combination of dry and wet etching is used to form the gate recess. Mushroom gate is dimensioned to 0.15um at AlGaAs surface through E-Beam photolithography technique. Threshold voltage is adjusted to be around 0V while Imax can be as high as 550mA/mm.

Wafers are thinned to 2mil thick for good thermal performance. Via are placed under source fingers to improve both electrical performances by reducing source inductance and also helps thermal performance by providing heat sink next to the hot spots.

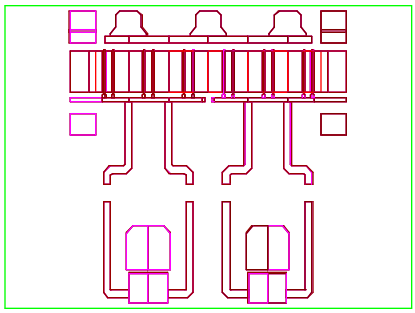

Fig. 1 1.2 mm Pre-matched Power Chip

PRODUCT DESIGN

Amplifier design is the result of trading off performance, cost, and application flexibility [Ref.3]. The most critical choice is the impedance matching circuit implementation. Options available include having no matching, partial matching, or full matching circuit implemented on chips. The chip can also have single or multiple stage of gain functions.

We made the choice of input-partially-matched power transistor design based on the following reasoning: High gain performance can be consistently obtained through on chip repeatable matching circuit. The highest power performance can only be obtained through matching circuits implemented on low loss ceramic substrates. Medium to low cost chips can be available by efficiently utilizing GaAs material mainly for active component instead of having all matching circuits on expensive Epi material. Finally, maximum chip application flexibility can be available by allowing the device to be partially matched instead of fully matched to enable re-tuning for any frequency within 6 GHz bandwidth of the center frequency.

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Electrical design aids are obtained from extensive device characterization, which includes four parts: DC, small signal, large signal, and load pull. From on wafer measured DC data, a gm vs. Vgs plot can be obtained, and quiescent bias point for initial test can be selected from the plot. After bench data was taken to confirm the best bias point for both gain and power needs, load pull is than performed at that bias point to obtain power and efficiency contours. Load pull result for a 400um device shows a complex load of mag 0.6 and angle 160 degree is best for P1dB and efficiency performance. This impedance level and associated performance is then confirmed using large signal simulation on HP MDS system.

The output matching circuit design based on results from load pull measurement is first implemented on 5 mil Al_2O_3 substrate with drain bond wires serving as part of the impedance transformer. After the load is optimized for power, the on chip input low pass LC circuit is then designed based on S parameters for maximum gain and stability analysis. Finally, large signal Root model is used to simulate amplifier power compression and two tones inter-modulation optimization.

Building block chips (Fig. 1) have 1.2 and 2.4 mm gate peripheral. Process evaluation has shown typical performance of 350mW/mm P-1dB and 9dB gain at 28GHz. Combining four of these cells (Fig. 2 & 3) at the output stage on carrier will have module performance of close to 34dBm. Driver stages are sized conservatively to ensure their being linear at all applications.

The final product (Fig. 4) includes four stage open module which is on a single CuW carrier, an output power detection function, and biasing stabilization and temperature sensing circuits which are on two pieces of PCB. All of these material combined with input isolator are fit into a 3"x 2" housing with waveguide connects.

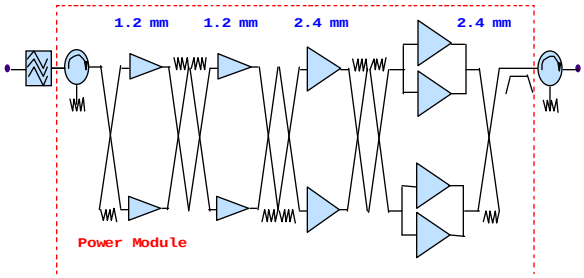

Fig. 2 Power Amplifier Topology

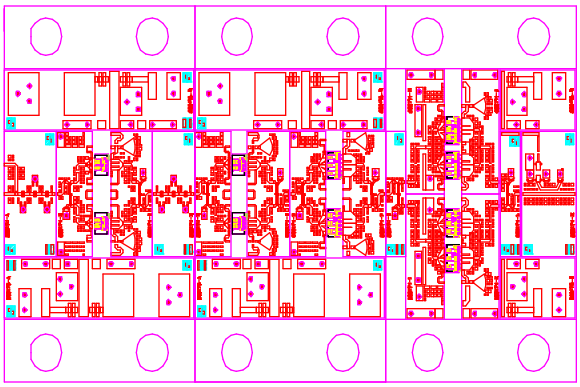

Fig. 3 Power Module Layout

Major mechanical consideration includes carrier, interface, and housing design.

Carrier design has been critical due to its high power nature. It has to be thick enough to avoid over temperature bow effect, which causes RF grounding problem. On the other end, it cannot be too thick to have the extra ground path at interface causing low performance. Our solution again compromised the two requirements. We have majority of the carrier be 50 mil thick for rigidity and stepped down to 25mil thick close to both RF ends to accommodate the shorter ground path need.

Our case design takes into consideration of both thin film hybrids as well as low cost PCB assembly for DC biasing and powers sensing. Thermal advantage from the heat sink tub process, spread out finger layout, and high thermal conductivity single piece package, all made this product cooler when used in the free run (without cooling fan) base station. The estimated thermal performance based on simulation as well as IR measurement shows a 45-degree C delta between flange and junction temperatures.

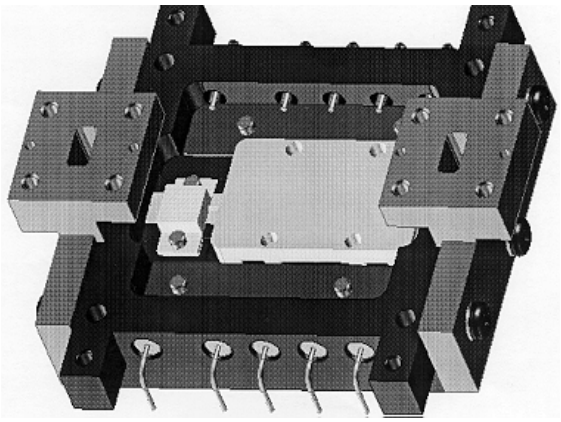

Fig. 4 Power Amplifier 3-D Drawing

PERFORMANCE

Chip performance measured on ten different wafers shows typically 29dBm P-1dB with 8.5dB linear gain can be obtained from the 2.4mm partially matched die at 28GHz while biased at Vd=5V and IdsQ=450mA.
Final products operate at 5V single power supply and at 45 degree C flange temperature. Four-stage module itself does exhibit close to 34dBm of P1dB. After this four-stage module is inserted into the case, overall amplifiers show 23dB of linear gain and 33 dBm (2W) of 1dB gain compression power for the entire 900 MHz bandwidth at 28 GHz (Fig. 5). This power and gain data is the statistics of the latest 10 amplifiers. Typical IMD3 at total output power of 1 watt is better than -28 dBc (Fig. 6).

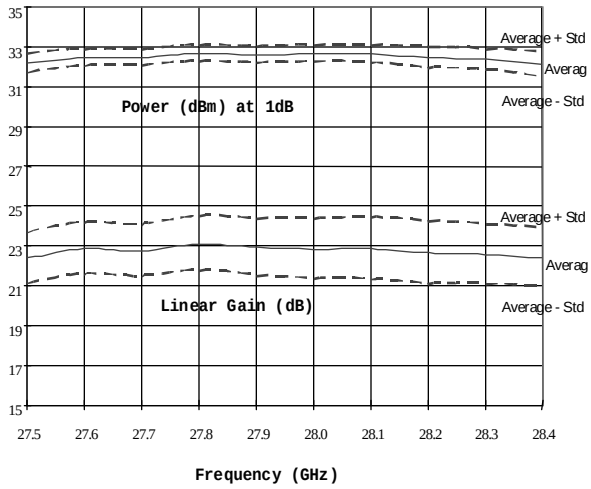

Fig. 5 Power and Gain Performance

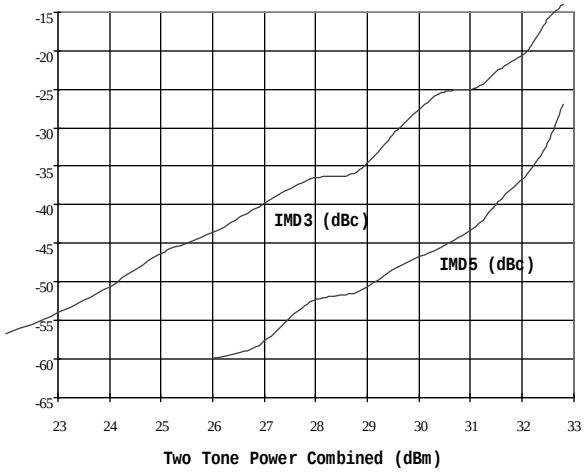

Fig.6 Typical Two Tone Inter-modulation

This amplifier is designed to meet the demanding hub station linearity requirement of DAVIC specification for grade A QPSK modulation of data and video transmission. When operated at 30dBm (1W) power output with single channel band limited signal, the spectral re-growth is -35dBc, 3dB better than the -32dBc performance target.

As to reliability, other than routine device reliability MTTF test that is in process, we have performed amplifier level operation life test. Three 2W amplifiers have been DC burned in at 85 degree C flange temperature. RF performance was constantly monitored. More than 1000 hours of data have been accumulated so far on these units and no noticeable degradation observed.

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CONCLUSION

A 2W SSPA based on advanced power PHEMT process has been developed for LMDS base station needs. Statistically analyzed result shows typical performance of 33dBm power and 23dB gain. Two-tone performances are typical IMD3 -28dBc when operated at 30dBm output power. When the unit is placed in customer's transmitter system and operated at 30dBm power output with single channel band limited signal, the spectral re-growth is -35dBc, 3dB better than the -32dBc performance target. To our knowledge, the linearity performance presented is the best reported so far for this application. This same design approach can be easily adapted to other high frequency, high power, and good linearity demand applications such as high power Ka band VSAT earth station needs.

ACKNOWELEDGE

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